SmartDV™

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SmartDV Broadens Support for Arm AMBA Protocol with Verification IP Solutions for AMBA CHI, CXS, LPI

Offerings include Verification IP, Synthesizable Transactors, Assertion IP

SAN JOSE, CALIF. — July 7, 2020 — SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Design and Verification Intellectual Property (IP), broadens its support for the Arm® AMBA® protocol with availability of Verification IP solutions for AMBA CHI, CXS and LPI protocols.

Today's announcement underscores SmartDV's commitment to the Arm developer community with an already extensive portfolio of earlier AMBA bus protocol solutions. Now available are AMBA CHI, CXS and LPI protocol Verification IP, assertion IP and SimXL™, Synthesizable Transactors for accelerating system-level, system-on-chip (SoC) testing on hardware emulators or field programmable gate array (FPGA) prototyping platforms.

"Arm AMBA protocols including CHI, CXS and LPI continue to be important components of high-performance, multi-processor SoCs," comments Deepak Kumar Tala, SmartDV's managing director. "Verification engineers require high-quality

Verification IP solutions for each of them to connect and manage an SoC's functional blocks, whether its coherent processors and high-performance interconnects, point-to-point communications or handling clock and power features. SmartDV meets this need so verification engineers can verify and debug their designs quickly, easily and more effectively."

SmartDV's proprietary, automated compiler-based technology ensures quick delivery of its offerings compliant with standard protocol specifications for new or evolving applications. Its Verification IP solutions are used throughout a coverage-driven chip design verification flow in simulation, emulation, FPGA prototyping and formal verification environments.

Included with all SmartDV's AMBA Verification IP are a configurable bus functional model (BFM), protocol monitor and library of integrated protocol checks. They support all major verification languages and methodologies, including the open verification methodology (OVM), universal verification methodology (UVM) and SystemC.

Availability and Pricing

The SmartDV Verification IP portfolio is available now and backed by an experienced R&D team who work individually with each user installation.

Pricing is available upon request.

Email requests for datasheets or more information should be sent to sales@Smart-DV.com.

SmartDV at Virtual DAC

SmartDV will exhibit virtually at the 57th Design Automation Conference (DAC) starting Monday, July 20, through Saturday, August 1. The Virtual Expo Hall will be open with Live Chat hours from 10:30 a.m. until 1:30 p.m. P.DT. Monday through Wednesday, July 20-22.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. SmartDV offers high-quality standard protocol Design and Verification IP for simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification and RISC-V CPU verification. Any of its Design and Verification IP solutions can be rapidly customized to meet specific customer design needs. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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